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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,505	07/22/2003	Terry Borer	015114-065900US	8087

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TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,505	BORER ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/22/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6,7,20-21,23,25,27-28,30-32,34,and 37- 38* is/are rejected.

7)☒ Claim(s) *2,4,5,8-19,22,24,26,29,33,35-36,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/02/04; 02/22/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/625,505 filed on 07/22/2003, claims 1-40 are pending.

Claim Objections

2. Claims 1, 30, 32, and 40 are objected to because of the following informalities: these claims contain unclear limitations, such as:

As claims 1 and 32: clarified " a series of values for each input parameter in a set of input parameter",

As claims 1 and 32: clarified what is "input parameter"?

As claims 1, 32, and 40: clarified the different between "output value" and "output metric".

~~As claim 30, line 2, term "the order" changes to "an order".~~

As claim 40: clarified " a series of values for each tuning parameter in a set of tuning parameter".

As claim 40: clarified what is "tuning parameter"?

As claim 40: clarified what is "exogenous noise"?

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 30-31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 30 and 31 recites the limitation "an order of configurations" in line 2 of claims 30 and 31. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. Claims 1 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Buch et al. (Buch) (US 5,550, 839).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **With respect to claims 1 and 32**, Buch discloses a method and computer system for compiling a design for an integrated circuit (fig. 7), the method comprising:

(code) automatically performing multiple compilations (fig. 7, Synopsys Design Compiler 108) of the design using a series of values for each input in a set of input parameters parameter (user constraints [144], timing constraint [148], modular verilog netlist [106], target libraries [112], and delay [124]) to generate output values for one or more output metrics (timing analysis report [132], constraint report [146], and converted verilog netlist [110]) (fig. 7);

(code) reporting the output values for the output metrics (timing analysis report [132], constraint report [146], and converted verilog netlist [110]) (fig. 7); and

(code) concluding the compilations when a stopping criteria has been reached (timing compare report [134] has to satisfy customer required [96]) (fig. 7).

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1, 3, 6-7, 20-21, 23, 25, 27-28, 32, 34, and 37-38 are rejected under 35 U.S.C. 102(e) as being anticipated by Dail et al. (Dai) (US 6,651,235).

10. **With respect to claims 1 and 32**, Dai discloses a method and computer system for compiling a design for an integrated circuit (col. 1, ll. 6-9 and col. 8, ll. 35-40), the method comprising:

(code for) automatically performing multiple compilations (fig. 10, netlist compiler [114]) of the design using a series of values for each input in a set of input parameters parameter (all the information before the steps netlist compiler [114] are input parameters, such as timing constraints or other constraints input) to generate output values for one or more output metrics (fig. 10, col. 12, ll. 29-34);

(code for) reporting the output values for the output metrics (col. 15, ll. 35-37); and

(code for) concluding the compilations when a stopping criteria has been reached (col. 15, ll. 37-45 and fig. 4, criteria met [66]).

11. **With respect to claims 3 and 34**, Dai discloses all the limitation of the set forth claims wherein the method produces a signature (size, shape and timing characteristic) of the best configuration of input parameters (how the cell formed in semiconductor substrate), for use in future compilations (thereafter consult the cell library when analyzing IC layout to the determine whether they meet the various timing constraints) (col. 12, ll. 39-49).

12. **With respect to claims 6 and 37**, Dai discloses the all the limitation of the set forth claims wherein one of the input parameters is a random seed or initial configuration parameter (predetermined lower limit) (col. 3, ll. 32-36 and ll. 47-62).

13. **With respect to claims 7 and 38**, Dai discloses the all the limitation of the set forth claims wherein one of the input parameters is effort level (time manner) for the compilation tool or a portion of the compilation tool (fig 3, col. 2, ll. 25-35, ll. 57-67, and col. 3, ll. 1-27).

14. **With respect to claim 20,** Dai discloses the method according to claim 1 wherein: the set of output metrics includes a minimum slack (delay) calculated on the integrated circuit (col. 2, ll. 43-56).

15. **With respect to claim 21,** Dai discloses the method according to claim 1 wherein: the set of output metrics includes a total slack (delay) calculated on the integrated circuit (fig. 14, col. 14, ll. 11-30 and ll. 47-64).

16. **With respect to claims 23 and 27-28,** Dai discloses the method according to claim 1 wherein: the stopping criteria is based on achieving a user's specified

constraints (--minimum signal delay or total signal delay--) (col. 16, ll. 5-16, col. 14, ll. 11-30 and ll. 47-64).

17. **With respect to claim 25,** Dai discloses the method according to claim 1 wherein: the stopping criteria is based on a number of failed constraints in the integrated circuit (col. 16, ll.17-24).

Allowable Subject Matter

18. Claim 40 would be allowable if rewritten or amended to overcome the Objection, set forth in this Office action.

19. The following is a statement of reasons for the indication of allowable subject matter: the prior does not teach or suggest the limitations: "concluding efficacy of the tuning parameter in the presence of exogenous"

20. Claims 2, 4-5, 8-19, 22, 24, 26, 29, 33, 35-36, and 39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. and rewritten the based claims to clarify the claim language as in above claim objections.

21. The following is a statement of reasons for the indication of allowable subject matter: the prior does not teach or suggest the limitations as listed:

As claims 2 and 33: "the method produces a table of results of the output metrics for each combination of input parameters used for a compilation".

As claims 4-5 and 35-36: "the method produces a metric of average results across a range of input parameters to indicate expected noise or variability".

As claims 8 and 39: "one of the input parameters modifies a default cost of a given resource for placement".

As claim 9: "one of the input parameters modifies a default soft-limit for fitting or synthesis".

As claim 10: "one of the input parameters modifies a coefficient indicating the speed versus resource usage optimization for the compilations".

As claim 11: "one of the input parameters defines a level of effort to a register packing algorithm that combines circuit elements in the design into fewer logic elements on the integrated circuit when enabled".

As claim 12: "one of the input parameters is a balancing parameter to technology mapping in synthesis."

As claim 13: "one of the input parameters adds or deletes one optimization algorithm or step from a default CAD flow, or modifies an order in which CAD steps are applied to the integrated circuit".

As claim 14: "one of the input parameters is a choice or specification of an alternate synthesis optimization script".

As claim 15: "one of the input parameters enables a netlist optimization or physical re-synthesis step".

As claim 16: "the set of output metrics include a measure of the longest delay path in the design".

As claim 17: "the set of output metrics includes a quantification of logic area or other resource usage of the integrated circuit".

As claim 18: "the set of output metrics includes an estimate of power consumption".

As claim 19: "the set of output metrics includes a metric for a number of paths, register-register pairs, IO- register pairs, or register-IO pairs that fail to meet a specified timing constraint".

As claim 22: "the stopping criteria for the method is based on exhausting all possible combination of specified input parameters independent of results".

As claim 24: "the stopping criteria is a total compile time consumed over all of the compilations thus far".

As claim 26: "the stopping criteria for the method is based on the number of failing timing paths in the circuit".

As claim 29: "the stopping criteria is based on a statistical calculation of possible success by the method.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nghia M. Doan
Patent Examiner
AU 2825
NMD

VUTHE SIEK
PRIMARY EXAMINER